4. Eliminating Failure Mechanisms in Advanced Packages

Course Leader: Darvin Edwards – Edwards Enterprises

Course Description:
Primary reliability failure mechanisms that plague semiconductor packages will be summarized along with solutions to enable faster qualification. The reliability of new package technologies such as heterogeneous package integration and chiplet technologies will be emphasized, as well as an overview of reliability issues in more traditional packages. Topics studied include reliability of Direct Cu Bonding (DCB), micro bump mechanical reliability, high density interconnect (HDI) reliability, TSV-chip interactions, electromigration performance, stress induced interlevel dielectric (ILD) damage under bumps and Cu pillars, saw induced ILD damage, solder joint reliability, the impact of aging on reliability performance and many more.

Primary failure analysis techniques will be described. For each failure mode, the resultant failure mechanisms and failure analysis techniques required to verify the mechanisms will be summarized. This solutions-focused course concentrates on key process parameters, design techniques and material selections that can eliminate failures and improve reliability, ensuring participants can design-in reliability and design-out failures for quicker time to market. The emphasis is on giving the student an intuitive understanding of the interaction between the various trade-offs, and providing the knowledge about the methodologies and tools needed to drive early evaluation of these reliability risks. Primary reliability failure mechanisms that plague semiconductor packages will be summarized along with solutions to enable faster qualification.

Course Outline:

1. Introduction to Package Reliability
2. Failure Modes vs. Failure Mechanisms
3. Failure Analysis Techniques
4. FC-BGA Package Failure Mechanisms
5. WLCSP Package Failure Mechanisms
6. Embedded Die & Fan-Out WLP/PLP Failure Mechanisms
7. TSV Failure Mechanisms
8. High Density Interconnection Reliability
9. Direct Bond Interconnect Reliability and Testing
10. Chiplet Challenges
11. Materials, Modeling, Design Rules and Reliability
12. Summary

Who Should Attend:
This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions.

Bio: Darvin formed Edwards' Enterprise Consulting LLC in 2014, specializing in helping companies solve package reliability and thermal problems, as well as providing training worldwide and patent litigation expertise. Current in-depth classes cover Heterogeneous Packaging Technologies, TSV and Fan-out Packages, Package Reliability, Package Materials, High Frequency Package Design, and Surface Mount Technologies.

Prior to forming Edwards' Enterprise Consulting, Darvin Edwards worked for Texas Instruments starting in 1980. There he developed integrated test structures to evaluate chip/package interactions, improved the thermal performance of TI's products, and led the Dallas package modeling team for fifteen years. He wrote design rules to ensure package reliability and helped develop flip-chip BGA, CSP, WCSP and TSVs technologies. Elected TI Fellow in 1999, he was responsible for Analog Si/Pkg interactions within the Semiconductor Packaging Group before retiring in 2013.

He has served four terms as Member at Large for the IEEE CPTM society and has been a member and alternately chair of the Electronics Components and Technology Conference Applied Reliability committee for 42 years. Darvin has authored and co-authored over 60 papers and articles covering IC packaging, has written three book chapters, and holds 26 US patents. He has been active with JEDEC, SRC, INEMI, and IMAPS.